ABSTRACT

A method and processor for shadow register array instruction processing are provided. Shadow register array control instructions are executed on data in a source array of registers to write the data simultaneously to a destination array of registers. The shadow array control instructions are available to perform context saving of the data during interrupt and non-interrupt processing. The shadow register array control instruction may write data stored in an array of primary registers to an array of shadow registers. Alternatively, the shadow register array control instruction may write data stored in an array of shadow registers to an array of primary registers.